# Masanori Hashimoto

Professor

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## Academic Qualifications

**Ph. D degree in Informatics** March 2001, Kyoto University, Kyoto, JAPAN

**M. E. degree** March 1999, Kyoto University, Kyoto, JAPAN

**B. E. degree** March 1997, Kyoto University, Kyoto, JAPAN

## Professional Experience

**Professor, Dept. Information Systems Engineering, Osaka University**
2016–present

**Associate Professor, Dept. Information Systems Engineering, Osaka University**
2004–2016

**Researcher of Japan Science and Technology Corporation**
2001–2005

**Research Associate, Dept. Communications & Computer Engineering, Kyoto University**
2001–2004

**Research Fellow of the Japan Society for the Promotion of Science**
2000–2001

## Research Area

VLSI design and design automation, especially

- Delay, power and signal integrity analysis
- Reconfigurable architecture

- Ultra low voltage design
- Reliable circuit design
- Reconfigurable architecture
- Soft error modeling and characterization
- Wireless sensor network and its applications
- On-chip high speed signaling
- Interconnect modeling
- Performance optimization in physical design

# Professional Activities and Service

- Member (2017, 2015), Technical Program Committee, IEEE Pacific Rim International Symposium on Dependable Computing (PRDC)
- Member (2016, 2015), Technical Program Committee, International Symposium on VLSI Design, Automation and Test (VLSI-DAT)
- Member (2016, 2015, 2014), Technical Program Committee, IEEE/ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)
- Member (2016, 2014), Technical Program Committee, IEEE International Test Conference (ITC)
- Member (2016, 2015, 2014, 2009, 2008, 2007), Technical Program Committee, IEEE/ACM Design Automation Conference (DAC)
- Member (2016, 2015, 2014), Technical Program Committee, Symposium on VLSI Circuits
- Subcommittee Chair (2015, 2014, 2013), Member (2012, 2011, 2009, 2008, 2007), Secretary (2006), Topic Chair (2004), Topic Co-Chair (2003), Technical Program Committee, IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC)
- Member (2016, 2015, 2014, 2013), Technical Program Committee, International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART)
- Member (2016, 2015, 2014, 2013), Technical Program Committee, China Semiconductor Technology International Conference
- Member (2016, 2015, 2009, 2008, 2006), Technical Program Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD)

- Member (2011, 2010, 2009, 2008, 2007, 2006), Technical Program Committee, IEEE/ACM International Conference on Computer Design (ICCD)
- Tutorial Vice Chair (2009), IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC)
- Member (2012, 2011), Technical Program Committee, IEEE/ACM Design Automation and Test Conference in Europe (DATE)
- Member (2012, 2011, 2010), Technical Program Committee, ACM International Symposium on Physical Design (ISPD)
- Member (2012, 2011, 2010, 2009, 2008, 2007), Technical Program Committee, IEEE International Symposium on Quality Electronic Design (ISQED)
- Publication Co-chair (2011), IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)
- Member (2009), Technical Program Committee, ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)
-
- Associate Editor (2015-2016), IEEE Transactions on VLSI Systems
- Associate Editor (2015), IEEE Transactions on Circuits and Systems I
- Associate Editor (2012-2015), IEICE Transactions on Fundamentals
- Guest Associate Editor (2015), Integration, the VLSI journal, Special Issue on VLSI Physical Design
- Guest Associate Editor (2016, 2015, 2014, 2013, 2012, 2011, 2010, 2009, 2008, 2007, 2005, 2004, 2003), Secretary (2006), IEICE Transactions on Fundamentals, Special Section on "VLSI Design and CAD Algorithm"
- Guest Associate Editor (2005), IEICE Transactions on Information and Systems, Special Section on "Recent Advances in Circuits and Systems"
- Guest Associate Editor (2009), IEICE Transactions on Electronics, Special Section on "Low-Leakage, Low-Voltage, Low-Power and High-Speed Technologies for System LSIs in Deep-Submicron Era"
- Secretary (2010), Guest Associate Editor (2012) IEICE Transactions on Electronics, Special Section on "Circuits and Design Techniques for Advanced Large Scale Integration"
- Guest Associate Editor (2015), IEICE Transactions on Electronics, Special Section on " Solid-State Circuit Design - Architecture, Circuit, Device and Design Methodology "

- Associate Editors-in-Chief (2013-), Associate Editor (2010-2012), IPSJ Transactions on System LSI Design Methodology
- 
- Secretary (2012), Technical Program Committee, JST International Symposium on Dependable VLSI Systems
- Secretary(2006–2008), Kansai Chapter, IEEE Circuits and Systems Society

# Honors and Awards

- IEEE Senior Member (2011)
- ”HISHO” The Top Thirty Young Researchers of Osaka University (2010)
- Special Feature Award, University LSI Design Contest, IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC) (2008)
- Outstanding Paper Award, Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) (2007)
- Best Paper Award, IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC) (2004)
- Ericsson Young Scientist Award (2002)
- Yamashita Memorial Award, Information Processing Society of Japan (2002)
- Young Investigator Award, IEICE (2000)
- Japan Chapter Award, IEEE Solid-State Circuit Society (1999)

# Professional Societies

- Senior Member, Institute of Electrrical and Electronics Engineerings (IEEE)
- Member, Association for Computing Machinery (ACM)
- Member, Institute of Electronics, Information and Communication Engineerings (IEICE)
- Member, Information Processing Society of Japan (IPSJ)

# Teaching

- Computer-Aided System-on-a-Chip Design
- Integrated System Architecture and Synthesis
- Computer System and Logic Design
- Fundamentals of Electronic Circuits I
- Exercise in Information Systems Engineering II

# Selected Publications

## Book

1. M. Hashimoto and R. Nair, Power Integrity for Nanoscale Integrated Systems, McGraw-Hill Professional, 2014.
2. M. Hashimoto and R. Nair, "Power Integrity Management in Integrated Circuits and Systems," Book chapter, Power Integrity Analysis and Management for Integrated Circuits, Prentice Hall PTR, May 2010.
3. R. Nair, M. Hashimoto, and N. Srivastava, "Ic Power Integrity and Optimal Power Delivery," Book chapter, Power Integrity Analysis and Management for Integrated Circuits, Prentice Hall PTR, May 2010.

## Journal

1. S. Iizuka, Y. Higuchi, M. Hashimoto, and T. Onoye, "Device-Parameter Estimation with Sensitivity-Configurable Ring Oscillator," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E98- A, no. 12, pp. 2607–2613, December 2015.
2. D. Fukuda, K. Watanabe, Y. Kanazawa, and M. Hashimoto, "Modeling the Effect of Global Layout Pattern on Wire Width Variation for On-The-Fly Etching Process Modification," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E98-A, no. 7, pp. 1467–1474, July 2015.
3. T. Shinada, M. Hashimoto, and T. Onoye, "Proximity Distance Estimation Based on Electric Field Communication between 1mm$^3$ Sensor Nodes," Analog Integrated Circuits and Signal Processing, May 2015.
4. S. Hirokawa, R. Harada, M. Hashimoto, and T. Onoye, "Characterizing Alpha- and Neutron-Induced SEU and MCU on SOTB and Bulk 0.4-V SRAMs," IEEE Transactions on Nuclear Science, vol. 62, no. 2, pp. 420–427, April 2015.

5. H. Konoura, D. Alnajjar, Y. Mitsuyama, H. Shimada, K. Kobayashi, H. Kanbara, H. Ochi, T. Imagawa, K. Wakabayashi, M. Hashimoto, T. Onoye, and H. Onodera, "Reliability-Configurable Mixed-Grained Reconfigurable Array Supporting C- Based Design and Its Irradiation Testing," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E97-A, no. 12, pp. 2518–2529, December 2014.

6. T. Amaki, M. Hashimoto, and T. Onoye, "A Process and Temperature Tolerant Oscillator-Based True Random Number Generator," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E97- A, no. 12, pp. 2393–2399, December 2014.

7. D. Fukuda, K. Watanabe, N. Idani, Y. Kanazawa, and M. Hashimoto, "Edge-Over -Erosion Error Prediction Method Based on Multi-Level Machine Learning Algorithm," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E97-A, no. 12, pp. 2373–2382, December 2014.

8. T. Uemura, T. Kato, R. Tanabe, H. Iwata, J. Ariyoshi, H. Matsuyama, and M. Hashimoto, "Exploring Well-Configurations for Minimizing Single Event Latchup," IEEE Transactions on Nuclear Science, vol. 61, no. 6, pp. 3282– 3289, December 2014.

9. H. Konoura, T. Kameda, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "NBTI Mitigation Method by Inputting Random Scan-In Vectors in Standby Time," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E97-A, no. 7, pp. 1483–1491, July 2014.

10. R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "SET Pulse-Width Measurement Suppressing Pulse-Width Modulation and Within-Die Process Variation Effects," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E97-A, no. 7, pp. 1461–1467, July 2014.

11. H. Fuketa, R. Harada, M. Hashimoto, and T. Onoye, "Measurement and Analysis of Alpha-Particle-Induced Soft Errors and Multiple Cell Upsets in 10T Subthreshold SRAM," IEEE Transactions on Device and Materials Reliability, vol. 14, no. 1, p. 463 – 470, March 2014.

12. D. Alnajjar, H. Konoura, Y. Ko, Y. Mitsuyama, M. Hashimoto, and T. Onoye, " Implementing Flexible Reliability in a Coarse Grained Reconfigurable Architecture," IEEE Transactions on VLSI Systems, vol. 21, no. 12, p. 2165 – 2178, December 2013.

13. T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Mitigating Multi-Bit- Upset with Well-Slits in 28 nm Multi-Bit-Latch," IEEE Transactions on Nuclear Science, vol. 60, no. 6, pp. 4362–4367, December 2013.

14. T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Soft-Error in Sram at Ultra-Low Voltage and Impact of Secondary Proton in Terrestrial Environment," IEEE Transactions on Nuclear Science, vol. 60, no. 6, pp. 4232–4237, December 2013.

15. K. Shinkai, M. Hashimoto, and T. Onoye, "A Gate-Delay Model Focusing on Current Fluctuation Over Wide Range of Process-Voltage-Temperature Variations," Integration, the VLSI Journal, vol. 46, no. 4, pp. 345–358, September 2013.

16. R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Impact of NBTI- Induced Pulse-Width Modulation on SET Pulse-Width Measurement," IEEE Transactions on Nuclear Science, vol. 60, no. 4, pp. 2630–2634, August 2013.

17. T.Kameda, H. Konoura, D. Alnajjar, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Field Slack Assessment for Predictive Fault Avoidance on Coarse-Grained Reconfigurable Devices," IEICE Trans. on Information and Systems , vol. E96 -D, no. 8, pp. 1624–1631, August 2013.

18. T. Amaki, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "A Worst-Case-Aware Design Methodology for Noise-Tolerant Oscillator-Based True Random Number Generator with Stochastic Behavior Modeling," IEEE Transactions on Information Forensics and Security, vol. 8, no. 8, pp. 1331–1342, August 2013.

19. Y. Ogasahara, M. Hashimoto, T. Kanamoto, and T. Onoye, "Supply Noise Suppression by Triple-Well Structure," IEEE Transactions on VLSI Systems, vol. 21, no. 4, pp. 781–785, April 2013.

20. D. Alnajjar, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Pvt-Induced Timing Error Detection Through Replica Circuits and Time Redundancy in Reconfigurable Devices," IEICE Electronics Express (ELEX), vol. 10, no. 5, April 2013.

21. T. Amaki, M. Hashimoto, and T. Onoye, "Jitter Amplifier for Oscillator- Based True Random Number Generator," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E96-A, no. 3, pp. 684–696, March 2013.

22. I. Homjakovs, T. Hirose, Y. Osaki, M. Hashimoto, and T. Onoye, "A 0.8-V 110 -Na Cmos Current Reference Circuit Using Subthreshold Operation," IEICE Electronics Express (ELEX), vol. 10, no. 4, March 2013.

23. I. Homjakovs, M. Hashimoto, T. Hirose, and T. Onoye, "Signal-Dependent Analog-To-Digital Conversion Based on Minimax Sampling," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E96- A, no. 2, pp. 459–468, February 2013.

24. T. Enami, T. Sato, and M. Hashimoto, "Power Distribution Network Optimization for Timing Improvement with Statistical Noise Model and Timing Analysis," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E95-A, no. 12, pp. 2261–2271, December 2012.

25. Y. Takai, M. Hashimoto, and T. Onoye, "Power Gating Implementation for Supply Noise Mitigation with Body-Tied Triple-Well Structure," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E95-A, no. 12, pp. 2220–2225, December 2012.

26. S. Kimura, M. Hashimoto, and T. Onoye, "A Body Bias Clustering Method for Low Test-Cost Post-Silicon Tuning," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E95-A, no. 12, pp. 2292–2300, December 2012.

27. R. Harada, S. Abe, H. Fuketa, T. Uemura, M. Hashimoto, and Y. Watanabe, " Angular Dependency of Neutron Induced Multiple Cell Upsets in 65-Nm 10t Subthreshold Sram," IEEE Transactions on Nuclear Science, vol. 59, no. 6, pp. 2791–2795, December 2012.

28. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Adaptive Performance Compensation with In-Situ Timing Error Predictive Sensors for Subthreshold Circuits," IEEE Transactions on VLSI Systems, vol. 20, no. 2, pp. 333–343, February 2012.

29. H. Konoura, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Stress Probability Computation for Estimating NBTI-Induced Delay Degradation," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E94- A, no. 12, pp. 2545–2553, December 2011.

30. K. Shinkai, M. Hashimoto, and T. Onoye, "Extracting Device-Parameter Variations with RO-Based Sensors," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E94-A, no. 12, pp. 2537–2544, December 2011.

31. T. Okumura and M. Hashimoto, "Setup Time, Hold Time and Clock-To-Q Delay Computation under Dynamic Supply Noise," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E94-A, no. 10, pp. 1948–1953, October 2011.

32. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Neutron-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," IEEE Transactions on Nuclear Science, vol. 58, no. 4, pp. 2097–2102, August 2011.

33. H. Fuketa, D. Kuroda, M. Hashimoto, and T. Onoye, "An Average-Performance- Oriented Subthreshold Processor Self-Timed by Memory Read Completion," IEEE Transactions on Circuits and Systems II, vol. 58, no. 5, pp. 299–303, May 2011.

34. S. Ninomiya and M. Hashimoto, "Accuracy Enhancement of Grid-Based SSTA by Coefficient Interpolation," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E93-A, no. 12, pp. 2441–2446, December 2010.

35. R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Measurement Circuits for Acquiring Set Pulse Width Distribution with Sub-FO1-Inverter-Delay Resolution," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E93-A, no. 12, pp. 2417–2423, December 2010.

36. T. Okumura, F. Minami, K. Shimazaki, K. Kuwada, and M. Hashimoto, "Gate Delay Estimation in STA under Dynamic Power Supply Noise," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E93- A, no. 12, pp. 2447–2455, December 2010.

37. T. Enami, K. Shinkai, S. Ninomiya, S. Abe, and M. Hashimoto, “Statistical Timing Analysis Considering Clock Jitter and Skew Due to Power Supply Noise and Process Variation,” IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E93-A, no. 12, pp. 2399–2408 , December 2010.

38. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, “Transistor Variability Modeling and Its Validation with Ring-Oscillation Frequencies for Body-Biased Subthreshold Circuits,” IEEE Transactions on VLSI Systems, vol. 18, no. 7, pp. 1118–1129, July 2010.

39. T. Kanamoto, T. Okumura, K. Furukawa, H. Takafuji, A. Kurokawa, K. Hachiya, T. Sakata, M. Tanaka, H. Nakashima, H. Masuda, T. Sato, and M. Hashimoto, “ Impact of Self-Heating in Wire Interconnection on Timing,” IEICE Trans. on Electronics, vol. E93-C, no. 3, pp. 388–392, March 2010.

40. K. Shinkai, M. Hashimoto, and T. Onoye, “Prediction of Self-Heating in Short Intra-Block Wires,” IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E93-A, no. 3, pp. 583–594, March 2010.

41. Z. Huang, A. Kurokawa, M. Hashimoto, T. Sato, M. Jiang, and Y. Inoue, “ Modeling the Overshooting Effect for CMOS Inverter Delay Analysis in Nanometer Technologies,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems , vol. 29, no. 2, pp. 250–260, February 2010.

42. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, “Trade-Off Analysis between Timing Error Rate and Power Dissipation for Adaptive Speed Control with Timing Error Prediction,” IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E92-A, no. 12, pp. 3094–3102, December 2009.

43. T. Sakata, T. Okumura, A. Kurokawa, H. Nakashima, H. Masuda, T. Sato, M. Hashimoto, K. Hachiya, K. Furukawa, M. Tanaka, H. Takafuji, and T. Kanamoto, “An Approach for Reducing Leakage Current Variation Due to Manufacturing Variability,” IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E92-A, no. 12, pp. 3016–3023, December 2009.

44. A. Kurokawa, T. Sato, T. Kanamoto, and M. Hashimoto, “Interconnect Modeling: a Physical Design Perspective (Invited),” IEEE Transactions on Electron Devices, vol.56, no.9, pp.1840–1851, September 2009.

45. Y. Ogasahara, M. Hashimoto, and T. Onoye, “All Digital Ring-Oscillator Based Macro for Sensing Dynamic Supply Noise Waveform,” IEEE Journal of Solid-State Circuits, vol.44, no.6, pp.1745–1755, June 2009.

46. T. Enami, S. Ninomiya, and M. Hashimoto, “Statistical Timing Analysis Considering Spatially and Temporally Correlated Dynamic Power Supply Noise,’ ’ IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems , vol.28, no.4, p.541 - 553, April 2009.

47. T. Okumura, A. Kurokawa, H. Masuda, T. Kanamoto, M. Hashimoto, H. Takafuji, H. Nakashima, N. Ono, T. Sakata, and T. Sato, "Improvement in Computational Accuracy of Output Transition Time Variation Considering Threshold Voltage Variations," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.92-A, no.4, pp.990–997, April 2009.

48. K. Hamamoto, H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "An Experimental Study on Body-Biasing Layout Style Focusing on Area Efficiency and Speed Controllability," IEICE Trans. on Electronics, vol.E92-C, no.2, pp.281–285, February 2009.

49. T. Kanamoto, Y. Ogasahara, K. Natsume, K. Yamaguchi, H. Amishiro, T. Watanabe, and M. Hashimoto, "Impact of Well Edge Proximity Effect on Timing, " IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E91-A, no.12, pp.3461-3464, December 2008.

50. S. Abe, M. Hashimoto, and T. Onoye, "Clock Skew Evaluation Considering Manufacturing Variability in Mesh-Style Clock Distribution," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E91-A, no.12, pp.3481-3487, December 2008.

51. M. Hashimoto, J. Siriporn, A. Tsuchiya, H. Zhu, and C.-K. Cheng, " Analytical Eye-Diagram Model for On-Chip Distortionless Transmission Lines and Its Application to Design Space Exploration," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E91-A, no.12, pp.3474-3480, December 2008.

52. Y. Mitsuyama, K. Takahashi, R. Imai, M. Hashimoto, T. Onoye, and I. Shirakawa, "Area-Efficient Reconfigurable Architecture for Media Processing, " IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E91-A, no.12, pp.3651-3662, December 2008.

53. M. Hashimoto, J. Yamaguchi, T. Sato, and H. Onodera, "Timing Analysis Considering Temporal Supply Voltage Fluctuation," IEICE Trans. on Information and Systems , vol.E91-D, no.3, pp.655–660, March 2008.

54. Y. Ogasahara, M. Hashimoto, and T. Onoye, "Measurement and Analysis of Inductive Coupling Noise in 90nm Global Interconnects," IEEE Journal of Solid-State Circuits, vol.43, no.3, pp.718–728, March 2008.

55. M. Hashimoto, J. Yamaguchi, T. Sato, and H. Onodera, "Timing Analysis Considering Temporal Supply Voltage Fluctuation," IEICE Trans. on Information and Systems, accepted for publication.

56. M. Hashimoto, J. Yamaguchi, and H. Onodera, "Timing Analysis Considering Spatial Power/Ground Level Variation," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E90-A, no.12, pp.2661 -2668, December 2007.

57. M. Hashimoto, T. Ijichi, S. Takahashi, S. Tsukiyama, and I. Shirakawa, " Transistor Sizing of LCD Driver Circuit for Technology Migration," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E90-A, no.12, pp.2712–2717, December 2007.

58. Y. Ogasahara, T. Enami, M. Hashimoto, T. Sato, and T. Onoye, "Validation of a Full-Chip Simulation Model for Supply Noise and Delay Dependence on Average Voltage Drop with On-Chip Delay Measurement," IEEE Trans. on CAS-II, vol.54, no.10, pp.868–872, October 2007.

59. A. Tsuchiya, M. Hashimoto, and H. Onodera, "Optimal Termination of On-Chip Transmission-Lines for High-Speed Signaling," IEICE Trans. on Electronics, vol.E90-C, no.6, pp.1267-1273, June 2007.

60. H. Kobayashi, N. Ono, T. Sato, J. Iwai, H. Nakashima, T. Okumura, and M. Hashimoto, "Proposal of Metrics for SSTA Accuracy Evaluation," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E90-A, no.4, pp.808–814, April 2007.

61. Y. Ogasahara, M. Hashimoto, and T. Onoye, "Quantitative Prediction of On- Chip Capacitive and Inductive Crosstalk Noise and Tradeoff between Wire Cross-Sectional Area and Inductive Crosstalk Effect," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E90-A, no.4, pp.724–731, April 2007.

62. A. Tsuchiya, M. Hashimoto, and H. Onodera, "Interconnect RL Extraction Based on Transfer Characteristics of Transmission-Line," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E89-A, no.12, pp.3585-3593, December 2006.

63. T. Kanamoto, T. Ikeda, A. Tsuchiya, H. Onodera, and M. Hashimoto, "Si- Substrate Modeling Toward Substrate-Aware Interconnect Resistance and Inductance Extraction in SoC Design," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E89-A, no.12, pp.3560 -3568, December 2006.

64. T. Sato, J. Ichimiya, N. Ono, and M. Hashimoto, "On-Chip Thermal Gradient Analysis Considering Interdependence between Leakage Power and Temperature,' ' IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E89-A, no.12, pp.3491-3499, December 2006.

65. T. Kanamoto, S. Akutsu, T. Nakabayashi, T. Ichinomiya, K. Hachiya, A. Kurokawa, H. Ishikawa, S. Muromoto, H. Kobayashi, and M Hashimoto, "Impact of Intrinsic Parasitic Extraction Errors on Timing and Noise Estimation," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E89-A, no.12, pp.3666-3670, December 2006.

66. S. Takahashi, S. Tsukiyama, M. Hashimoto, and I. Shirakawa, "A Sampling Switch Design Procedure for Active Matrix Liquid Crystal Displays," IEICE Trans. on Fundamentals of

Electronics, Communications and Computer Sciences, vol.E89-A, no.12, pp.3538-3545, December 2006.

67. T. Sato, M. Hashimoto, and H. Onodera, "Successive Pad Assignment for Minimizing Supply Voltage Drop," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E88-A,, no.12, pp. 3429-3436, December 2005.

68. T. Sato, J. Ichimiya, N. Ono, K. Hachiya, and M. Hashimoto, "On-Chip Thermal Gradient Analysis and Temperature Flattening for SoC Design," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E88-A, no.12, pp.3382-3389, December 2005.

69. A. Kurokawa, M. Hashimoto, A. Kasebe, Z.-C. Huang, , Y. Yang, Y. Inoue, R. Inagaki, and H. Masuda, "Second-Order Polynomial Expressions for On-Chip Interconnect Capacitance," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E88-A, no.12, pp.3453-3462, December 2005.

70. M. Hashimoto, T. Yamamoto, and H. Onodera, "Statistical Analysis of Clock Skew Variation in H-Tree Structure," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E88-A, no.12, pp.pp. 3375-3381, December 2005.

71. A. Muramatsu, M. Hashimoto, and H. Onodera, "Effects of On-Chip Inductance on Power Distribution Grid," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E88-A, no.12, pp.3564-3572, December 2005.

72. A. Tsuchiya, M. Hashimoto, and H. Onodera, "Performance Limitation of On- Chip Global Interconnects for High-Speed Signaling," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E88-A, no.4, pp.885-891, April 2005.

73. T. Miyazaki, M. Hashimoto, and H. Onodera, "A Performance Prediction of Clock Generation PLLs: a Ring Oscillator Based PLL and an LC Oscillator Based PLL," IEICE Trans. on Electronics, vol.E88-C, no.3, pp.437-444, March 2005.

74. M. Hashimoto and H. Onodera, "Crosstalk Noise Optimization by Post-Layout Transistor Sizing," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E87-A, no.12, pp.3251-3257, December 2004.

75. M. Hashimoto, Y. Yamada, and H. Onodera, "Equivalent Waveform Propagation for Static Timing Analysis," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems , vol.23, no.4, pp.498-508, April 2004.

76. A. Tsuchiya, M. Hashimoto, and H. Onodera, "Representative Frequency for Interconnect R(f)L(f)C Extraction," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E86-A, no.12, pp.2942 -2951, December 2003.

77. M. Hashimoto, Y. Hayashi, and H. Onodera, "Experimental Study on Cell-Base High-Performance Datapath Design," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E86-A, no.12, pp.3204 -3207, December 2003.

78. M. Hashimoto, M. Takahashi, and H. Onodera, "Crosstalk Noise Estimation for Generic Rc Trees," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E86-A, no.12, pp.2965-2973, December 2003.

79. M. Hashimoto and H. Onodera, "Increase in Delay Uncertainty by Performance Optimization," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E85-A, no.12, pp.2799-2802, December 2002.

80. M. Hashimoto and H. Onodera, "Post-Layout Transistor Sizing for Power Reduction in Cell-Base Design," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E84-A, no.11, pp.2769-2777, November 2001.

81. M. Hashimoto and H. Onodera, "A Performance Optimization Method by Gate Resizing Based on Statistical Static Timing Analysis," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E83-A, no.12, pp.2558-2568, December 2000.

82. M. Hashimoto, H. Onodera, and K. Tamaru, "A Power and Delay Optimization Method Using Input Reordering in Cell-Based CMOS Circuits," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol.E82-A, no.1, pp.159-166, January 1999.

## International Conference

1. Y. Masuda, M. Hashimoto, and T. Onoye, "Measurement of Timing Error Detection Performance of Software-Based Error Detection Mechanisms and Its Correlation with Simulation," ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), March 2016.

2. R. Doi, J. Hotate, T. Kishimoto, T. Higashi, H. Ochi, M. Tada, T. Sugibayashi, K. Wakabayashi, H. Onodera, Y. Mitsuyama, and M. Hashimoto, " Highly-Dense Mixed Grained Reconfigurable Architecture with Via-Switch," ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), March 2016.

3. U. Schlichtmann, M. Hashimoto, I. H.-R. Jiang, and B. Li, "Reliability, Adaptability and Flexibility in Timing: Buy a Life Insurance for Your Circuits (Invited)," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 705–711, January 2016.

4. N. Banno, M.Tada, K. Okamoto, N. Iguchi, T. Sakamoto, M. Miyamura, Y. Tsuji, H. Hada, H. Ochi, H. Onodera, M. Hashimoto, and T. Sugibayashi, "A Novel Two-Varistors (a-Si/SiN/a-Si) Selected Complementary Atom Switch (2V-1CAS) for Nonvolatile Crossbar

Switch with Multiple Fan-Outs," Technical Digest of IEEE International Electron Devices Meeting (IEDM), pp. 32–35, December 2015.

5. Y. Masuda, M. Hashimoto, and T. Onoye, "Performance Evaluation of Software- Based Error Detection Mechanisms for Localizing Electrical Timing Failures under Dynamic Supply Noise," Proceedings of International Conference on Computer-Aided Design (ICCAD), pp. 315-322, November 2015.

6. R. Doi, M. Hashimoto, and T. Onoye, "An Analytic Evaluation on Soft Error Immunity Enhancement Due to Temporal Triplication," Proceedings of IEEE Pacific Rim International Symposium on Dependable Computing (PRDC), November 2015.

7. S. Iizuka, Y. Masuda, M. Hashimoto, and T. Onoye, "Stochastic Timing Error Rate Estimation under Process and Temporal Variations," Proceedings of International Test Conference (ITC), October 2015.

8. Y. Akihara, T. Hirose, Y. Tanaka, N. Kuroki, M. Numa, and M. Hashimoto, "A Wireless Power Transfer System for Small-Sized Sensor Applications," Proceedings of International Conference on Solid State Devices and Materials (SSDM), pp. 154–155, September 2015.

9. S. Hirokawa, R. Harada, M. Hashimoto, K. Sakuta, and Y. Watanabe, "Neutron- Induced SEU and MCU Rate Characterization and Analysis of SOTB and Bulk SRAMs at 0.3V Operation," IEEE Nuclear and Space Radiation Effects Conference (NSREC), July 2015.

10. M. Ueno, M. Hashimoto, and T. Onoye, "Real-Time On-Chip Supply Voltage Sensor and Its Application to Trace-Based Timing Error Localization," Proceedings of International On-Line Testing Symposium (IOLTS), pp. 188– 193, July 2015.

11. M. Hashimoto, "Run-Time Performance Adaptation: Opportunities and Challenges (Invited)," Proceedings of IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), June 2015.

12. T. Uemura, T. Kato, S. Okano, H. Matsuyama, and M. Hashimoto, "Impact of Package on Neutron Induced Single Event Upset in 20 nm SRAN," Proceedings of International Symposium on Reliability Physics (IRPS), April 2015.

13. T. Uemura and M. Hashimoto, "Investigation of Single Event Upset and Total Ionizing Dose in FeRAM for Medical Electronic Tag," Proceedings of International Symposium on Reliability Physics (IRPS), April 2015.

14. T. Uemura, S. Okano, T. Kato, H. Matsuyama, and M. Hashimoto, "Soft Error Immune Latch Design for 20 nm Bulk CMOS," Proceedings of International Reliability Physics Symposium (IRPS), April 2015.

15. S. Ukawa, T. Shinada, M. Hashimoto, Y. Itoh, and T. Onoye, "3D Node Localization from Node-To-Node Distance Information Using Cross-Entropy Method," Proceedings of Virtual Reality Conference (VR), March 2015.

16. S. Iizuka, Y. Higuchi, M. Hashimoto, and T. Onoye, "Area Efficient Device- Parameter Estimation Using Sensitivity-Configurable Ring Oscillator," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 731–736, January 2015.

17. M. Hashimoto, D. Alnajjar, H. Konoura, Y. Mitsuyama, H. Shimada, K. Kobayashi, H. Kanbara, H. Ochi, T. Imagawa, K. Wakabayashi, T. Onoye, and H. Onodera, "Reliability-Configurable Mixed-Grained Reconfigurable Array Compatible with High-Level Synthesis," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 14–15, January 2015.

18. T. Amaki, M. Hashimoto, and T. Onoye, "An Oscillator-Based True Random Number Generator with Process and Temperature Tolerance," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 4–5, January 2015.

19. M. Hashimoto, "Stochastic Verification of Run-Time Performance Adaptation with Field Delay Testing (Invited)," Proceedings of Asia Pacific Conference on Circuits and Systems (APCCAS), pp. 751–754, November 2014.

20. M. Hashimoto, "Opportunities and Verification Challenges of Run-Time Performance Adaptation (Invited)," Proceedings of Asian Test Symposium (ATS), pp. 248–253, November 2014.

21. M. Hashimoto, "Toward Robust Subthreshold Circuit Design: Variability and Soft Error Perspective (Invited)," Proceedings of SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), October 2014.

22. A. Iokibe, M. Hashimoto, and T. Onoye, "Feasibility Evaluation on an Instant Invader Detection System with Ultrasonic Sensors Scattered on the Ground," Proceedings of International Conference on Sensing Technology (ICST), pp. 188–193, September 2014.

23. T. Uemura, T. Kato, R. Tanabe, H. Iwata, J. Ariyoshi, H. Matsuyama, and M. Hashimoto, "Optimizing Well-Configuration for Minimizing Single Event Latchup," IEEE Nuclear and Space Radiation Effects Conference (NSREC), July 2014.

24. R. Harada, S. Hirokawa, and M. Hashimoto, "Measurement of Alpha- and Neutron-Induced SEU and MCU on SOTB and Bulk 0.4 V SRAMs," IEEE Nuclear and Space Radiation Effects Conference (NSREC), July 2014.

25. T. Uemura, T. Kato, R. Tanabe, H. Iwata, H. Matsuyama, M. Hashimoto, K. Takahisa, M. Fukuda, and K. Hatanaka, "Preventing Single Event Latchup with Deep P-Well on P-Substrate," Proceedings of International Reliability Physics Symposium (IRPS), June 2014.

26. M. Ueno, M. Hashimoto, and T. Onoye, "Trace-Based Fault Localization with Supply Voltage Sensor," ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), pp. 77–81, March 2014.

27. H. Konoura, D. Alnajjar, Y. Mitsuyama, H. Ochi, T. Imagawa, S. Noda, K. Wakabayashi, M. Hashimoto, and T. Onoye, "Mixed-Grained Reconfigurable Architecture Supporting Flexible Reliability and C-Based Design," Proceedings of International Conference on ReConFigurable Computing and FPGAs (ReConFig), December 2013.

28. S. Iizuka, M. Mizuno, D. Kuroda, M. Hashimoto, and T. Onoye, "Stochastic Error Rate Estimation for Adaptive Speed Control with Field Delay Testing," Proceedings of International Conference on Computer-Aided Design (ICCAD), pp. 107–114, November 2013.

29. J. Kono, M. Hashimoto, and T. Onoye, "Feasibility Evaluation of Near-Field Communication in Clay with 1-$mm^3$ Antenna," Proceedings of Asia-Pacific Microwave Conference (APMC), pp. 1121–1123, November 2013.

30. T. Amaki, M. Hashimoto, and T. Onoye, "A Process and Temperature Tolerant Oscillator-Based True Random Number Generator with Dynamic 0/1 Bias Correction," Proceedings of IEEE Asian Solid-State Circuits Conference (A- SSCC), pp. 133–136, November 2013.

31. D. Alnajjar, H. Konoura, Y. Mitsuyama, H. Shimada, K. Kobayashi, H. Kanbara, H. Ochi, T. Imagawa, S. Noda, K. Wakabayashi, M. Hashimoto, T. Onoye, and H. Onodera, "Reliability-Configurable Mixed-Grained Reconfigurable Array Supporting C-To-Array Mapping and Its Radiation Testing," Proceedings of IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 313–316, November 2013.

32. R. Harada, M. Hashimoto, and T. Onoye, "NBTI Characterization Using Pulse- Width Modulation," IEEE/ACM Workshop on Variability Modeling and Characterization, November 2013.

33. M. Hashimoto, "Soft Error Immunity of Subthreshold SRAM (Invited)," Proceedings of IEEE International Conference on ASIC, pp. 91–94, October 2013.

34. T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Scaling Trend of Sram and Ff of Soft-Error Rate and Their Contribution to Processor Reliability on Bulk Cmos Technology," IEEE Nuclear and Space Radiation Effects Conference (NSREC), July 2013.

35. T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Soft-Error in SRAM at Ultra Low Voltage and Impact of Secondary Proton in Terrestrial Environment, " IEEE Nuclear and Space Radiation Effects Conference (NSREC), July 2013.

36. T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Mitigating Multi-Cell- Upset with Well-Slits in 28nm Multi-Bit-Latch," IEEE Nuclear and Space Radiation Effects Conference (NSREC), July 2013.

37. T. Shinada, M. Hashimoto, and T. Onoye, "Proximity Distance Estimation Based on Capacitive Coupling between 1mm3 Sensor Nodes," Proceedings of International NEWCAS Conference, June 2013.

38. M. Ueno, M. Hashimoto, and T. Onoye, "Real-Time Supply Voltage Sensor for Detecting/Debugging Electrical Timing Failures," Proceedings of Reconfigurable Architectures Workshop (RAW), pp. 301–305, May 2013.

39. Y. Higuchi, K. Shinkai, M. Hashimoto, R. Rao, and S. Nassif, "Extracting Device-Parameter Variations Using a Single Sensitivity-Configurable Ring Oscillator," Proceedings of IEEE European Test Symposium (ETS), pp. 106– 111, May 2013.

40. M. Hashimoto, "Robust Subthreshold Circuit Design to Manufacturing and Environmental Variability (Invited)," China Semiconductor Technology International Conference (CSTIC), pp. 1079–1084, March 2013.

41. D. Alnajjar, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Static Voltage Over -Scaling and Dynamic Voltage Variation Tolerance with Replica Circuits and Time Redundancy in Reconfigurable Devices," Proceedings of International Conference on ReConFigurable Computing and FPGAs (ReConFig), December 2012.

42. I. Homjakovs, M. Hashimoto, T. Hirose, and T. Onoye, "Signal-Dependent Analog-To-Digital Converter Based on MINIMAX Sampling," Proceedings of International SoC Design Conference (ISOCC), p. 120 – 123 , November 2012.

43. R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Impact of NBTI-Induced Pulse-Width Modulation on SET Pulse-Width Measurement," Proceedings of European Conference on Radiation and Its Effects on Components and Systems (RADECS), September 2012.

44. T. Kameda, H. Konoura, D. Alnajjar, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "A Predictive Delay Fault Avoidance Scheme for Coarse-Grained Reconfigurable Architecture," Proceedings of International Conference on Field Programmable Logic and Applications (FPL) , August 2012.

45. R. Harada, S. Abe, H. Fuketa, T. Uemura, M. Hashimoto, and Y. Watanabe, " Angular Dependency of Neutron Induced Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," IEEE Nuclear and Space Radiation Effects Conference, July 2012.

46. R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "SET Pulse-Width Measurement Eliminating Pulse-Width Modulation and Within-Die Process Variation Effects," Proceedings of International Reliability Physics Symposium (IRPS), April 2012.

47. S. Kimura, M. Hashimoto, and T. Onoye, "Body Bias Clustering for Low Test- Cost Post-Silicon Tuning," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 283–289, February 2012.

48. H. Konoura, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Implications of Reliability Enhancement Achieved by Fault Avoidance on Dynamically Reconfigurable Architecture," Proceedings of International Conference on Field Programmable Logic and Applications (FPL) , pp. 189–194, September 2011.

49. Y. Takai, M. Hashimoto, and T. Onoye, "Power Gating Implementation for Noise Mitigation with Body-Tied Triple-Well Structure," Proceedings of IEEE Custom Integrated Circuits Conference (CICC), September 2011.

50. T. Kameda, H. Konoura, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "NBTI Mitigation by Giving Random Scan-In Vectors during Standby Mode," Proceedings of International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS), pp. 152–161, September 2011.

51. M. Hashimoto and H. Fuketa, " Adaptive Performance Compensation with On- Chip Variation Monitoring (Invited)," Proceedings of International Midwest Symposium on Circuits and Systems (MWSCAS), August 2011.

52. I. Homjakovs, M. Hashimoto, T. Hirose, and T. Onoye, "Signal-Dependent Analog-To-Digital Conversion Based on MINIMAX Sampling," Proceedings of International Midwest Symposium on Circuits and Systems (MWSCAS), August 2011.

53. T. Amaki, M. Hashimoto, and T. Onoye, "An Oscillator-Based True Random Number Generator with Jitter Amplifier," Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), pp. 725–728, May 2011.

54. R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Neutron Induced Single Event Multiple Transients with Voltage Scaling and Body Biasing," Proceedings of International Reliability Physics Symposium (IRPS), pp. 253 –257, April 2011.

55. S. Kimura, M. Hashimoto, and T. Onoye, "Body Bias Clustering for Low Test- Cost Post-Silicon Tuning," ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), pp. 46–51, April 2011.

56. K. Shinkai, M. Hashimoto, and T. Onoye, "Extracting Device-Parameter Variations with RO-Based Sensors," ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), pp. 13 –18, March 2011.

57. D. Alnajjar, H. Kounoura, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "MTTF Measurement under Alpha Particle Radiation in a Coarse-Grained Reconfigurable Architecture with Flexible Reliability," IEEE Workshop on Silicon Errors in Logic - System Effects, March 2011.

58. K. Shinkai and M. Hashimoto, "Device-Parameter Estimation with On-Chip Variation Sensors Considering Random Variability," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 683–688, January 2011.

59. T. Amaki, M. Hashimoto, and T. Onoye, "Jitter Amplifier for Oscillator- Based True Random Number Generator," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 81–82, January 2011.

60. M. Hashimoto, "Run-Time Adaptive Performance Compensation Using On-Chip Sensors (Invited)," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 285–290, January 2011.

61. Y. Takai, M. Hashimoto, and T. Onoye, "Evaluation of Power Gating Structures Focusing on Power Supply Noise with Measurement and Simulation," Proceedings of IEEE Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), pp. 213–216, October 2010.

62. T. Okumura and M. Hashimoto, "Setup Time, Hold Time and Clock-To-Q Delay Computation under Dynamic Supply Noise," Proceedings of IEEE Custom Integrated Circuits Conference (CICC), September 2010.

63. T. Amaki, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "A Design Procedure for Oscillator-Based Hardware Random Number Generator with Stochastic Behavior Modeling," Proceedings of International Workshop on Information Security Applications (WISA), August 2010.

64. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Alpha-Particle- Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM, " Proceedings of International Reliability Physics Symposium (IRPS), pp. 213–217, May 2010.

65. S. Abe, K. Shinkai, M. Hashimoto, and T. Onoye, "Clock Skew Reduction by Self-Compensating Manufacturing Variability with On-Chip Sensors," ACM Great Lake Symposium on VLSI (GLSVLSI), pp. 197–202, May 2010.

66. Y. Takai, Y. Ogasahara, M. Hashimoto, and T. Onoye, "Measurement of On-Chip I/O Power Supply Noise and Correlation Verification between Noise Magnitude and Delay Increase Due to SSO," Proceedings of IEEE Workshop on Signal Propagation on Interconnects (SPI), pp. 19–20, May 2010.

67. D. Kuroda, H. Fuketa, M. Hashimoto, and T. Onoye, "A 16-Bit RISC Processor with 4.18pJ/Cycle at 0.5V Operation," Proceedings of IEEE COOL Chips, p. 190, April 2010.

68. H. Konoura, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Comparative Study on Delay Degrading Estimation Due to NBTI with Circuit/Instance/Transistor- Level Stress Probability Consideration," Proceedings of International Symposium on Quality Electronic Design (ISQED), pp. 646–651, March 2010.

69. R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Measurement Circuits for Acquiring SET Pulse Width Distribution with Sub-FO1-Inverter-Delay Resolution," Proceedings of International Symposium on Quality Electronic Design (ISQED), pp. 839–844, March 2010.

70. T. Enami, K. Shinkai, S. Ninomiya, S. Abe, and M. Hashimoto, "Statistical Timing Analysis Considering Clock Jitter and Skew Due to Power Supply Noise and Process Variation," ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), pp. 41–46, March 2010.

71. S. Abe, K. Shinkai, M. Hashimoto, and T. Onoye, "Clock Skew Reduction by Self-Compensating Manufacturing Variability with On-Chip Sensors," ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), pp. 89–94, March 2010.

72. T. Okumura, F. Minami, K. Shimazaki, K. Kuwada, and M. Hashimoto, "Gate Delay Estimation in STA under Dynamic Power Supply Noise," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), p. 775 – 780, January 2010.

73. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Adaptive Performance Control with Embedded Timing Error Predictive Sensors for Subthreshold Circuits," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), p. 361 – 362, January 2010.

74. D. Alnajjar, Y. Ko, T. Imagawa, M. Hiromoto, Y. Mitsuyama, M. Hashimoto, H. Ochi, and T. Onoye, "Soft Error Resilient Vlsi Architecture for Signal Processing," Proceedings of IEEE International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), pp. 183–186, December 2009.

75. S. Ninomiya and M. Hashimoto, " Enhancement of Grid-Based Spatially- Correlated Variability Modeling for Improving SSTA Accuracy," Proceedings of IEEE International SOC Conference (SOCC), pp. 337–340, September 2009.

76. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Adaptive Performance Compensation with In-Situ Timing Error Prediction for Subthreshold Circuits, " Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp. 215–218, September 2009.

77. K. Hamamoto, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Tuning-Friendly Body Bias Clustering for Compensating Random Variability in Subthreshold Circuits," Proceedings of IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), pp. 51–56, August 2009.

78. D. Alnajjar, Y. Ko, T. Imagawa, H. Konoura, M. Hiromoto, Y. Mitsuyama, M. Hashimoto, H. Ochi, and T. Onoye, "Coarse-Grained Dynamically Reconfigurable Architecture with Flexible Reliability," Proceedings of International Conference on Field Programmable Logic and Applications (FPL), pp. 186–192, August 2009.

79. S. Watanabe, M. Hashimoto, and T. Sato, "A Case for Exploiting Complex Arithmetic Circuits Towards Performance Yield Enhancement," Proceedings of International Symposium on Quality Electronic Design (ISQED), pp. 401–407, March 2009.

80. Y. Ko, D. Alnajjar, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Coarse- Grained Dynamically Reconfigurable Architecture with Flexible Reliability," Proceedings of Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), pp.236–241, March 2009.

81. D. Alnajjar, Y. Ko, T. Imagawa, M. Hiromoto, Y. Mitsuyama, M. Hashimoto, H. Ochi, and T. Onoye, "A Coarse-Grained Dynamically Reconfigurable Architecture Enabling Flexible Reliability," Proceedings of IEEE Workshop on System Effects of Logic Soft Errors (SELSE), March 2009.

82. K. Shinkai and M. Hashimoto, "A Gate Delay Model Over Wide-Range of Process and Environmental Variability," ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), pp.79- -84, February 2009.

83. L. Zhang, Y. Zhang, A. Tsuchiya, M. Hashimoto, E. Kuh, and C-K Cheng, "High Performance On-Chip Differential Signaling Using Passive Compensation for Global Communication," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.385–390, January 2009.

84. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Trade-Off Analysis between Timing Error Rate and Power Dissipation for Adaptive Speed Control with Timing Error Prediction," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.266-271, January 2009.

85. T. Enami, M. Hashimoto, and T. Sato, "Decoupling Capacitance Allocation for Timing with Statistical Noise Model and Timing Analysis," Proceedings of ACM/IEEE International Conference on Computer-Aided Design (ICCAD), pp.420 –425, November 2008.

86. Y. Ogasahara, M. Hashimoto, T. Kanamoto, and T. Onoye, "Measurement of Supply Noise Suppression by Substrate and Deep N-Well in 90nm Process," Proceedings of IEEE Asian Solid-State Circuits Conference (A-SSCC), pp.397 –400, November 2008.

87. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Vth Variation Modeling and Its Validation with Ring Oscillation Frequencies for Body- Biased Circuits and Subthreshold Circuits," Proceedings of Workshop on Test Structure Design for Variability Characterization, November 2008.

88. Y. Zhang, L. Zhang, A. Tsuchiya, M. Hashimoto, and C.-K. Cheng, "On-Chip High Performance Signaling Using Passive Compensation," Proceedings of IEEE International Conference on Computer Design (ICCD), pp.182-187, October 2008.

89. H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Correlation Verification between Transistor Variability Model with Body Biasing and Ring Oscillation Frequency in 90nm Subthreshold Circuits," Proceedings of IEEE/ ACM International Symposium on Low Power Electronics and Design (ISLPED), pp.3–8, August 2008.

90. S. Watanabe, M. Hashimoto, and T. Sato, "Cascading Dependent Operations for Mitigating Timing Variability," Proceedings. of Workshop on Quality-Aware Design (W-QUAD), June 2008.

91. S. Takahashi, S. Tsukiyama, M. Hashimoto, and I. Shirakawa, "A Design Method of Finding Optimal Sampling Pulse and Transistor Size in a Sampling Circuit for Liquid Crystal Displays," In Proceedings of International Technical Conference on Circuits/Systems, Computers and Communications (ITC- CSCC), June 2008.

92. K. Hamamoto, H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, " Experimental Study on Body-Biasing Layout Style – Negligible Area Overhead Enables Sufficient Speed Controllability –," Proceedings of ACM Great Lake Symposium on VLSI (GLSVLSI), pp.387–390, May 2008.

93. T. Enami, S. Ninomiya, and M. Hashimoto, "Statistical Timing Analysis Considering Spatially and Temporally Correlated Dynamic Power Supply Noise,' ' Proceedings of ACM International Symposium on Physical Design (ISPD), pp. 160-167, April 2008.

94. S. Abe, M. Hashimoto, and T. Onoye, "Clock Skew Evaluation Considering Manufacturing Variability in Mesh-Style Clock Distribution," Proceedings of International Symposium on Quality Electronic Design (ISQED), pp.520–525, March 2008.

95. Y. Ogasahara, M. Hashimoto, and T. Onoye, "Dynamic Supply Noise Measurement Circuit Composed of Standard Cells Suitable for In-Site Soc Power Integrity Verification," Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.107–108, January 2008.

96. K. Hamamoto, H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "A Study on Body-Biasing Layout Style Focusing on Area Efficiency and Speed," Proceedings of Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), pp.233-237, October 2007.

97. M. Hashimoto, J. Siriporn, A. Tsuchiya, H. Zhu, and Chung-Kuan Cheng, " Analytical Eye-Diagram Model for On-Chip Distortionless Transmission Lines and Its Application to Design Space Exploration," Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp.869–872, September 2007.

98. T. Kanamoto, Y. Ogasahara, K. Natsume, K. Yamaguchi, H. Amishiro, T. Watanabe, and M. Hashimoto, "Impact of Well Edge Proximity Effect on Timing, " Proceedings of 37th European Solid-State Device Research Conference (ESSDERC), pp.115–118, September 2007.

99. Y. Ogasahara, M. Hashimoto, and T. Onoye, "Dynamic Supply Noise Measurement with All Digital Gated Oscillator for Evaluating Decoupling Capacitance Effect," Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp.783–786, September 2007.

100. K. Shinkai, M. Hashimoto, and T. Onoye, "Future Prediction of Self-Heating in Short Intra-Block Wires," In Proceedings of International Symposium on Quality Electronic Design (ISQED), pp.660-665, March 2007.

101. K. Shinkai, M. Hashimoto, A. Kurokawa, and T. Onoye, “A Gate Delay Model Focusing on Current Fluctuation Over Wide-Range of Process and Environmental Variability,” In Proceedings of ACM/IEEE International Conference on Computer-Aided Design (ICCAD), pp.47-53, November 2006.

102. Y. Ogasahara, M. Hashimoto, and T. Onoye, “Quantitative Prediction of On- Chip Capacitive and Inductive Crosstalk Noise and Discussion on Wire Cross- Sectional Area Toward Inductive Crosstalk Free Interconnects,” In Proceedings of IEEE International Conference on Computer Design (ICCD), pp. 70-75, October 2006.

103. Y. Ogasahara, M. Hashimoto, and T. Onoye, “Measurement of Inductive Coupling Effect on Timing in 90nm Global Interconnects,” In Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp.721-724, September 2006.

104. Y. Ogasahara, T. Enami, M. Hashimoto, T. Sato, and T. Onoye, “Measurement Results of Delay Degradation Due to Power Supply Noise Well Correlated with Full-Chip Simulation,” In Proceedings of IEEE Custom Integrated Circuits Conference (CICC),, pp.861-864, September 2006.

105. T. Ijichi, M. Hashimoto, S. Takahashi, S. Tsukiyama, and I. Shirakawa, “ Transistor Sizing of Lcd Driver Circuit for Technology Migration,” In Proceedings of International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC), vol.1, p.I25-I28, July 2006.

106. T. Kanamoto, T. Ikeda, A. Tsuchiya, H. Onodera, and M. Hashimoto, “Si- Substrate Modeling Toward Substrate-Aware Interconnect Resistance and Inductance Extraction in SoC Design,” In Proceedings of IEEE Wrokshop on Signal Propagation on Interconnects (SPI), pp.227-230, May 2006.

107. K. Shinkai, M. Hashimoto, A. Kurokawa, and T. Onoye, “A Gate Delay Model Focusing on Current Fluctuation Over Wide-Range of Process Variations,” In ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), pp.59-64, February 2006.

108. A. Tsuchiya, M. Hashimoto, and H. Onodera, “Interconnect Rl Extraction at a Single Representative Frequency,” In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.515-520, January 2006.

109. T. Kanamoto, T. Ikeda, A. Tsuchiya, H. Onodera, and M. Hashimoto, “ Effective Si-Substrate Modeling for Frequency-Dependent Interconnect Resistance and Inductance Extraction,” In Proceedings of International Workshop on Compact Modeling (IWCM), pp.51-56, January 2006.

110. S. Takahashi, A. Taji, S. Tsukiyama, M. Hashimoto, and I. Shirakawa, “A Sampling Switch Design for Liquid Crystal Displays,” In Proceedings of IEEE International Region 10 Conference, no.1C-03.3, November 2005.

111. T. Kouno, M. Hashimoto, and H. Onodera, “Input Capacitance Modeling of Logic Gates for Accurate Static Timing Analysis,” In Proceedings of IEEE Asian Solid-State Circuits Conference (A-SSCC), pp.453-456, November 2005.

112. S. Uemura, T. Miyazaki, M. Hashimoto, and H. Onodera, “Estimation of Maximum Oscillation Frequency for CMOS LCVCO,” In Proceedings of IEEJ International Analog VLSI Workshop, October 2005.

113. M. Hashimoto, A. Tsuchiya, A. Shinmyo, and H. Onodera, “Performance Prediction of On-Chip High-Throughput Global Signaling,” In Proceedings of IEEE 14th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP), pp.79-82, October 2005.

114. A. Tsuchiya, M. Hashimoto, and H. Onodera, “Design Guideline for Resistive Termination of On-Chip High-Speed Interconnects,” In Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp.613-616, September 2005.

115. Y. Ogasahara, M. Hashimoto, and T. Onoye, “Measurement and Analysis of Delay Variation Due to Inductive Coupling,” In Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp.305-308, September 2005.

116. S. Takahashi, A. Taji, S. Tsukiyama, M. Hashimoto, and I. Shirakawa, “A Design Scheme for Sampling Switch in Active Matrix LCD,” In Proceedings of European Conference on Circuit Theory and Design, no.3e-212, August 2005.

117. A. Tsuchiya, M. Hashimoto, and H. Onodera, “Substrate Loss of On-Chip Transmission-Lines with Power/Ground Wires in Lower Layer,” In Proceedings of IEEE Workshop on Signal Propagation on Interconnects (SPI), pp.201-202, May 2005.

118. Y. Uchida, S. Tani, M. Hashimoto, S. Tsukiyama, and I. Shirakawa, “ Interconnect Capacitance Extraction for System LCD Circuits,” In Proceedings of Great Lakes Symposium on VLSI (GLSVLSI), pp.160-163, April 2005.

119. A. Tsuchiya, M. Hashimoto, and H. Onodera, “Effects of Orthogonal Power/ Ground Wires on On-Chip Interconnect Characteristics,” In Proceedings of International Meeting for Future of Electron Devices, Kansai, pp.33-34, April 2005.

120. A. Muramatsu, M. Hashimoto, and H. Onodera, “Effects of On-Chip Inductance on Power Distribution Grid,” In Proceedings of International Symposium on Physical Design (ISPD), pp.63-69, April 2005.

121. M. Hashimoto, T. Yamamoto, and H. Onodera, “Statistical Analysis of Clock Skew Variation in H-Tree Structure,” In Proceedings of International Symposium on Quality Electronic Design (ISQED), pp.402-407, March 2005.

122. A. Shinmyo, M. Hashimoto, and H. Onodera, “Design and Measurement of 6.4 Gbps 8:1 Multiplexer in 0.18um CMOS Process,” In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), p.D9-D10, January 2005.

123. T. Sato, N. Ono, J. Ichimiya, K. Hachiya, and M. Hashimoto, "On-Chip Thermal Gradient Analysis and Temperature Flattening for SoC Design," In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.1074-1077, January 2005.

124. T. Sato, M. Hashimoto, and H. Onodera, "Successive Pad Assignment Algorithm to Optimize Number and Location of Power Supply Pad Using Incremental Matrix Inversion," In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.723-728, January 2005.

125. M. Hashimoto, J. Yamaguchi, T. Sato, and H. Onodera, "Timing Analysis Considering Temporal Supply Voltage Fluctuation," In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.1098-1101, January 2005.

126. A. Tsuchiya, M. Hashimoto, and H. Onodera, "Return Path Selection for Loop Rl Extraction," In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.1078-1081, January 2005.

127. M. Hashimoto, A. Tsuchiya, A. Shinmyo, and H. Onodera, "Performance Prediction of On-Chip Global Signaling," In IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) , pp.87-100, November 2004. (Invited talk)

128. M. Hashimoto, J. Yamaguchi, and H. Onodera, "Timing Analysis Considering Spatial Power/Ground Level Variation," In Proceedings of ACM/IEEE International Conference on Computer-Aided Design (ICCAD), pp.814-820, November 2004.

129. T. Sato, M. Hashimoto, and H. Onodera, "An Ir-Drop Minimization by Optimizing Number and Location of Power Supply Pads," In Proceedings of Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), pp.66-72, October 2004.

130. M. Hashimoto, T. Yamamoto, and H. Onodera, "Statistical Analysis of Clock Skew Variation," In Proceedings of Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), pp.214-219, October 2004.

131. T. Miyazaki, M. Hashimoto, and H. Onodera, "A Performance Prediction of Clock Generation PLLs: a Ring Oscillator Based PLL and an LC Oscillator Based PLL," In IEEJ International Analog VLSI Workshop, pp.45-50, October 2004.

132. M. Hashimoto, A. Tsuchiya, and H. Onodera, "On-Chip Global Signaling by Wave Pipelining," In IEEE 13th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP), pp.311-314, October 2004.

133. A. Muramatsu, M. Hashimoto, and H. Onodera, "Lsi Power Network Analysis with On-Chip Wire Inductance," In Proceedings of Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), pp.55-60, October 2004.

134. A. Tsuchiya, M. Hashimoto, and H. Onodera, "Performance Limitation of On- Chip Global Interconnects for High-Speed Signaling," In Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp.489-492, September 2004.

135. A. Shinmyo, M. Hashimoto, and H. Onodera, "Design and Optimization of CMOS Current Mode Logic Dividers," In IEEE Asia-Pacific Conference on Advanced System Integrated Circuits , pp.434-435, August 2004.

136. M. Hashimoto, K. Fujimori, and H. Onodera, "Automatic Generation of Standard Cell Library in Vdsm Technologies," In Proceedings of International Symposium on Quality Electronic Design (ISQED), pp.36-41, March 2004.

137. A. Tsuchiya, M. Hashimoto, and H. Onodera, "Representative Frequency for Interconnect R(f)L(f)C Extraction," In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.691-696, January 2004.

138. T. Miyazaki, M. Hashimoto, and H. Onodera, "A Performance Comparison of PLLs for Clock Generation Using Ring Oscillator VCO and LC Oscillator in a Digital CMOS Process," In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.545-546, January 2004.

139. M. Hashimoto, Y. Yamada, and H. Onodera, "Equivalent Waveform Propagation for Static Timing Analysis," In Proceedings of ACM/IEEE International Conference on Computer-Aided Design (ICCAD), pp.169-175, November 2003.

140. M. Hashimoto, Y. Yamada, and H. Onodera, "Capturing Crosstalk-Induced Waveform for Accurate Static Timing Analysis," In Proceedings of ACM/IEEE International Symposium on Physical Design (ISPD), pp.18-23, April 2003.

141. Y. Yamada, M. Hashimoto, and H. Onodera, "Slew Calculation Against Diverse Gate-Input Waveforms for Accurate Static Timing Analysis," In Proceedings of Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), pp.280-287, April 2003.

142. A. Tsuchiya, M. Hashimoto, and H. Onodera, "Frequency Determination for Interconnect Rlc Extraction," In Proceedings of Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), pp.288-293, April 2003.

143. T. Sato, T. Kanamoto, A. Kurokawa, Y. Kawakami, H. Oka, T. Kitaura, H. Kobayashi, and M. Hashimoto, "Accurate Prediction of the Impact of On-Chip Inductance on Interconnect Delay Using Electrical and Physical Parameters," In Proceedings of Asia and South Pacific Design Automation Conference (ASP- DAC), pp.149-155, January 2003.

144. M. Hashimoto, K. Fujimori, and H. Onodera, "Standard Cell Libraries with Various Driving Strength Cells for 0.13, 0.18 and 0.35um Technologies," In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.589-590, January 2003.

145. M. Hashimoto, D. Hiramatsu, A. Tsuchiya, and H. Onodera, "Interconnect Structures for High-Speed Long-Distance Signal Transmission," In Proceedings of IEEE International ASIC/SoC Conference, pp.426-430, September 2002.

146. M. Hashimoto, Y. Hayashi, and H. Onodera, “Experimental Study on Cell-Base High-Performance Datapath Design,” In Proceedings of IEEE/ACM International Workshop on Logic & Synthesis (IWLS), pp.283-287, June 2002.

147. M. Hashimoto, M. Takahashi, and H. Onodera, “Crosstalk Noise Optimization by Post-Layout Transistor Sizing,” In Proceedings of ACM/IEEE International Symposium on Physical Design (ISPD), pp.126-130, April 2002.

148. A. Tsuchiya, M. Hashimoto, and H. Onodera, “Driver Sizing for High- Performance Interconnects Considering Transmission-Line Effects,” In roceedings of Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), pp.377-381, October 2001.

149. M. Takahashi, M. Hashimoto, and H. Onodera, “Crosstalk Noise Estimation for Generic Rc Trees,” In Proceedings of International Conference on Computer Design (ICCD), pp.110-116, September 2001.

150. H. Onodera, M. Hashimoto, and T. Hashimoto, “Asic Design Methodology with On-Demand Library Generation,” In Proceedings of Symposium on VLSI Circuits, pp.57-60, June 2001.

151. M. Hashimoto and H. Onodera, “Increase in Delay Uncertainty by Performance Optimization,” In Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), vol.V, pp.379-382, May 2001.

152. M. Hashimoto and H. Onodera, “Post-Layout Transistor Sizing for Power Reduction in Cell-Based Design,” In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp.359-365, January 2001.

153. M. Hashimoto and H. Onodera, “A Statistical Delay-Uncertainty Analysis of the Circuits Path-Balanced by Gate/Transistor Sizing,” In Proceedings of ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), pp.34-37, December 2000.

154. T. Iwahashi, T. Shibayama, M. Hashimoto, K. Kobayashi, and H. Onodera, “ Vector Quantization Processor for Mobile Video Communication,” In Proceedings of IEEE International ASIC/SoC Conference, pp.75-79, September 2000.

155. M. Hashimoto and H. Onodera, “A Performance Optimization Method by Gate Resizing Based on Statistical Static Timing Analysis,” In Proceedings of the Ninth Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), pp.115-121, April 2000.

156. M. Hashimoto and H. Onodera, “A Performance Optimization Method by Gate Sizing Using Statistical Static Timing Analysis,” In Proceedings of ACM International Symposium on Physical Design (ISPD), pp.111-116, April 2000.

157. M. Hashimoto, H. Onodera, and K. Tamaru, “Practical Gate Resizing Technique Considering Glitch Reduction for Low Power Design,” In Proceedings of the 36th IEEE/ACM Design Automation Conference (DAC), pp.446-451, January 1999.

158. M. Hashimoto, H. Onodera, and K. Tamaru, “A Power Optimization Method Considering Glitch Reduction by Gate Sizing,” In Proceedings of IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), pp. 221-226, August 1998.

159. M. Hashimoto, H. Onodera, and K. Tamaru, “Input Reordering for Power and Delay Optimization,” In Proceedings of IEEE International ASIC Conference and Exhibit, pp.194-198, September 1997.